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Substitute for form 1449A/B/PTO				Complete If Known	
				Application Number	10/768,971
				Filing Date	January 30, 2004
				First Named Inventor	Franz Hofmann
				Art Unit	N/A 2815
				Examiner Name	Not Yet Assigned <i>Woot</i>
Sheet	1	of	1	Attorney Docket Number	20046/0200815-US0

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)	MM-DD-YYYY		
67	AA	US-6,252,284-B1	06-26-2001	Muller et al.	

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Country Code <sup>3</sup> -Number-Kind Code <sup>4</sup> (if known)	MM-DD-YYYY		

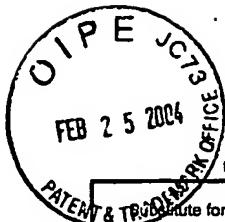
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Examiner Signature	<i>E01</i>	Date Considered	<i>8-25-05</i>
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Information Disclosure Statement by Applicant <i>(Use as many sheets as necessary)</i>				Complete If Known	
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ED	AA	US-4,996,574-B1	02-26-1991	Shirasaki	
	AB	US-5,300,455-B1	04-05-1994	Vuillermoz et al.	
	AC	US-5,623,155-B1	04-22-1997	Kerber et al.	
	AD	US-5,915,183-B1	06-22-1999	Gambino et al.	
	AE	US-6,091,076-B1	07-18-2000	Deleonibus	
	AF	US-6,207,511-B1	03-27-2001	Chapman et al.	

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ED	CA	Fujiwara, A. et al: "Suppression of Unintentional Formation of Parasitic SI Islands on ASI Single-Electron Transistor by the Use of Sin Masked Oxidation"; Extended Abstracts of the 1997 International Conference on Solid State Devices and Materials, Japan Society of Applied Physics. Tokyo, Japan, 1 September 1997, pages 482-483.			
	CB	Ishii, T. et al: "Characterization of One-Dimensional Conduction in an Ultra-Thin Poly-Si Wire"; Extended Abstracts of the International Conference on Solid State Devices and Materials", Japan Society of Applied Physics. Tokyo, Japan, 21 August 1995, pages 201-203.			
	CC	Hisamoto, Digh et al: "A Fully Depleted Lean-Channel Transistor (DELTA) - A Novel Vertical Ultrathin SOI MOSFET"; IEEE Electron Device Letters, Vol. 11, No. 1, January 1990, pages 36-38.			
	CD	Hisamoto, Digh et al: "A Folded-Channel MOSFET for Deep-sub-tenth Micron Era"; IEDM 98, pages 1032-1034, 1998.			
ED	CE	Kedzierski, Jakub et al: "Complementary silicide source/drain thin-body MOSFETS for the 20nm gate length regime"; IEDM 2000, pages 57-60.			

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